Attorney Docket No.: 5580-04402

REMARKS

Applicant respectfully requests reconsideration of the subject application as amended. In response to the Office Action mailed 3/24/05, Applicant is filing this amendment. Claims 1, 2, 4, 5, 10-12, 14, 15, 17, 18, 23-25 and 27 are still pending.

In the Office Action mailed 3/24/05, the Examiner has rejected claims 1, 2, 4, 5, 14, 15, 17, 18 and 27 under 35 U.S.C. §103(a) as being unpatentable over Riordan et al (U.S. Patent 5,027,270; Riordan) in view of Eisen et al. (U.S. Patent 5,897,654; Eisen) and claims 10-12 and 23-25 under 35 U.S.C. §103(a) as being unpatentable over Riordan in view of Eisen and further in view of Merchant et al. (U.S. Patent 6,665,792; Merchant). Applicant submits that none of the relied upon references teach the claimed embodiments of the invention as amended.

Riordan discloses a processor controlled interface between a processor, instruction cache and main memory. In the event of a cache miss, the main memory address generated by the processor is transferred to the memory interface and the processor enters a stall mode to halt instruction processing (see for example, Riordan at col. 3, lines 31-38). The embodiments of the present invention, as now recited in the amended independent claims, recite the detection of a replay of an instruction in a load/store pipeline due to a load miss. The stall state is then applied to the load/store pipeline, as well as to one or more other pipelines, by comparing a destination register corresponding to the instruction causing the load miss to other instructions in the queue for dependencies to the load miss. The miss tag corresponds to the destination register of the instruction causing the load miss and when the miss tag and the fill tag comparison results in a match, the pipelines exit the stall state. Riordan fails to disclose these aspects of the claimed embodiments of the invention.

In regards to Eisen and Merchant, Eisen discloses fetching from a cache during a cache fill operation and Merchant discloses a processor having a replay system. However, Eisen and Merchant fail to disclose the recited claim elements as noted in the paragraph directly above.

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Accordingly, Applicant submits that Riordan, Eisen and Merchant, singly or combined, fail to disclose the embodiments of the invention as now recited in the amended claims.

Accordingly, Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. §103(a) rejection and allow pending claims 1, 2, 4, 5, 10-12, 14, 15, 17, 18, 23-25 and 27, as amended.

If there are any fee shortages related to this response, please charge such fee shortages to Deposit Account No. 50-2126.

Respectfully submitted,

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